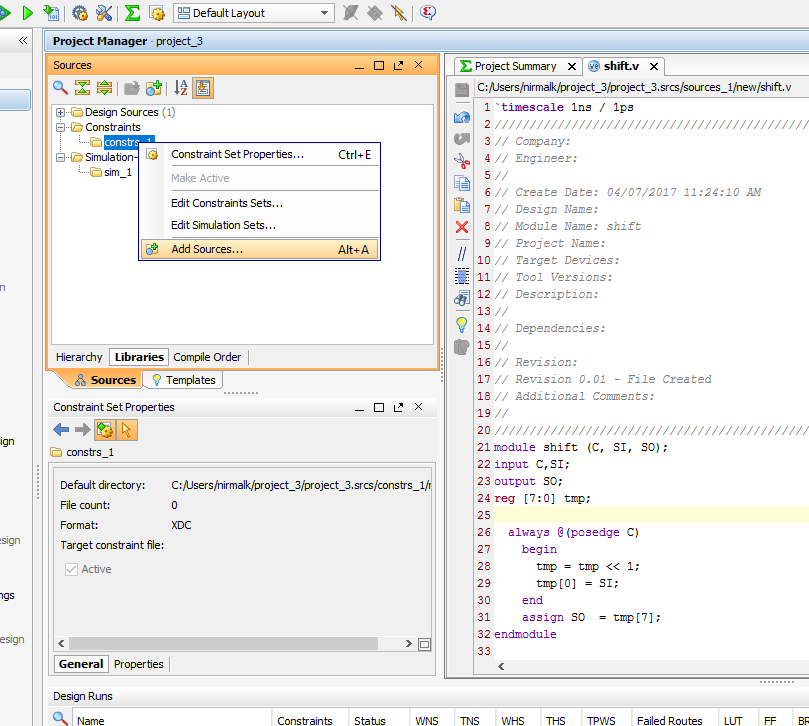
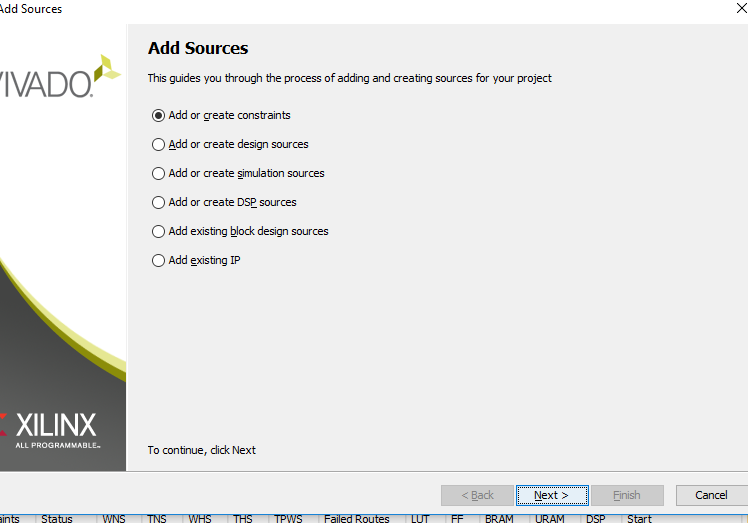
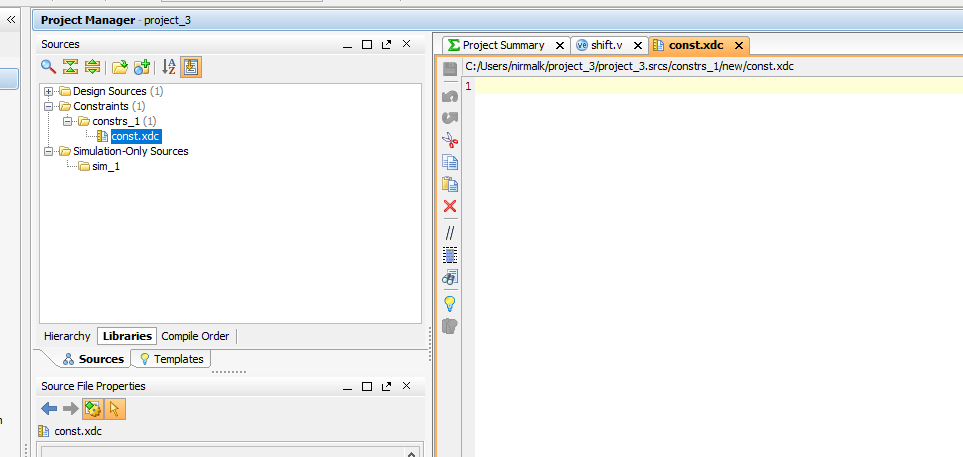
**How to set up Timing constraint to determine operating frequency of your design.**

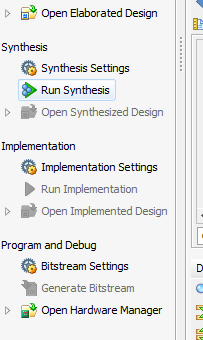
1. Create empty constraint file (const.xdc) for the design



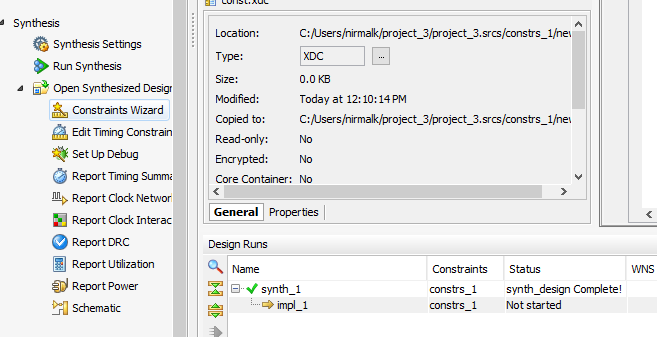




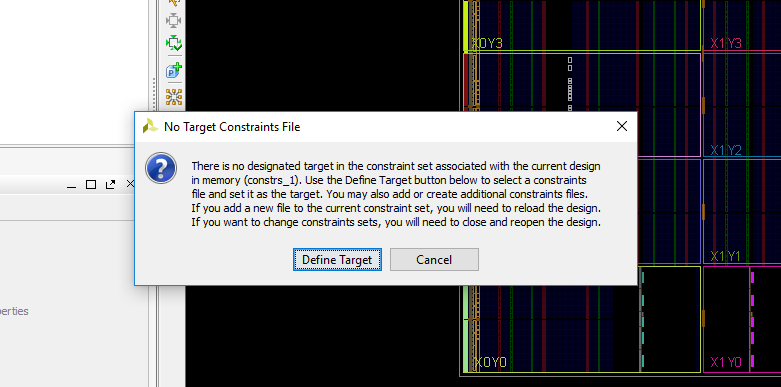
1. Synthesize design.



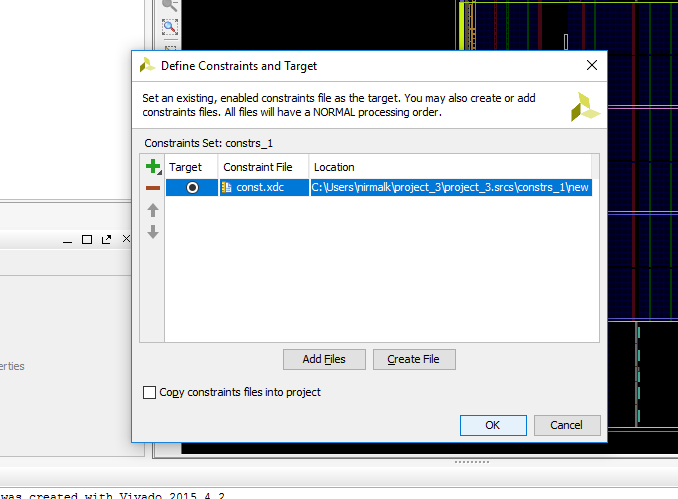
1. After synthesis is done, do not continue to implementation. Expand the tab “Open Synthesized Design” and click on “constraints wizard”.



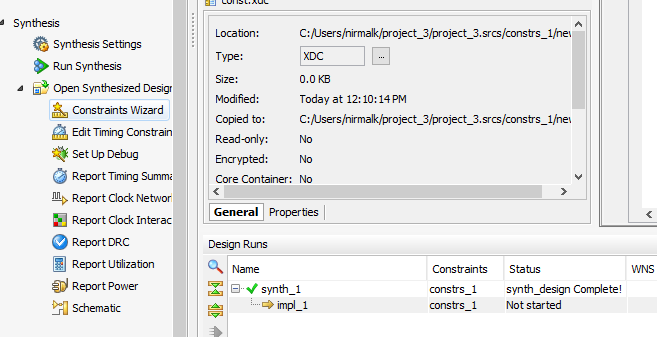
1. We need to set target constraint file. Click on “Define Target” on following window.



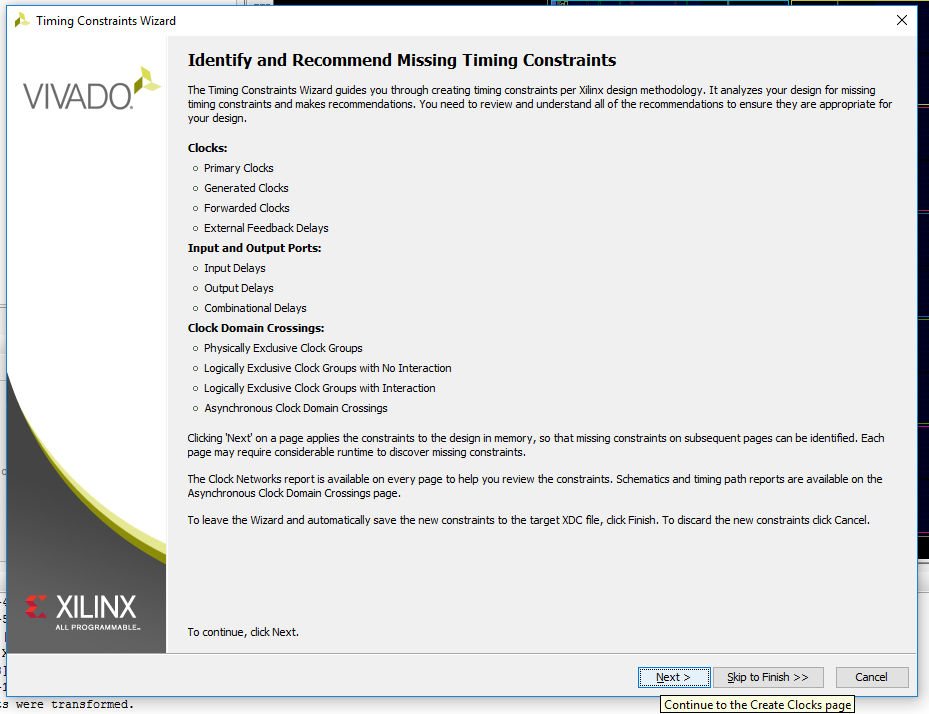
1. Select “const.xdc” as target constraint file and click ok.



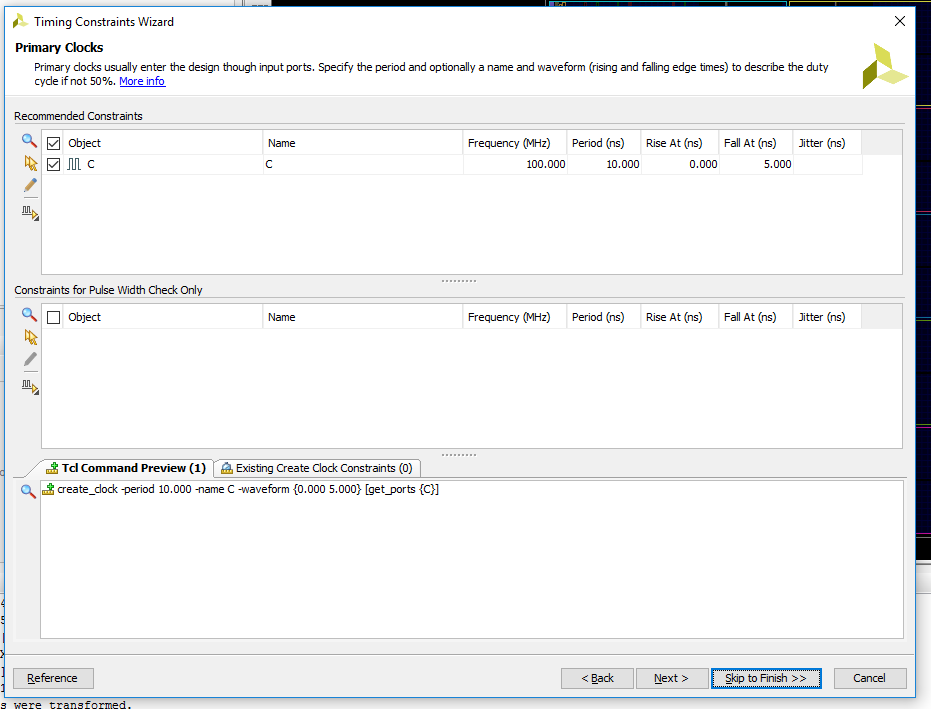
1. Again click on “Constraints wizard”.



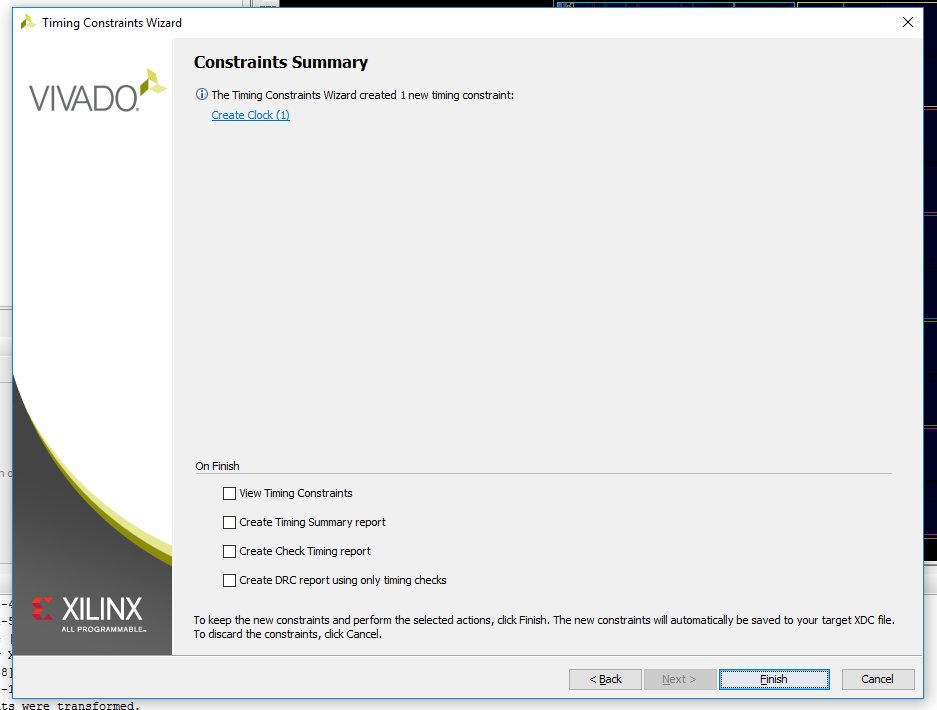
1. After clicking you will get following GUI. Click on Next to set up the constraint on clock.



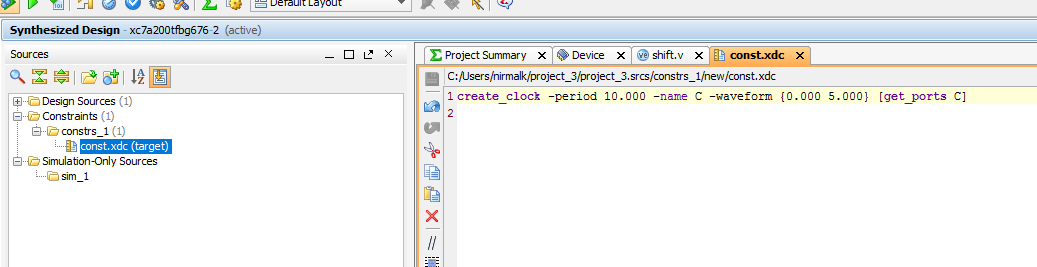
1. Select “clock” on which you want to set the constraint. In following figure clock “C” is selected and set to be run on 100 Mhz. You can click Next to see what other constraint you can set or click on “Skip to finish”.



1. Select finish in the GUI.



1. Reopen the const.xdc to check the constraint on the clock. It contains “create\_clock -period 10.000 -name C -waveform {0.000 5.000} [get\_ports C]”. Which means clock “C” period is “10 ns”, i.e. frequency is 100 MHz. “{0.000 5.000}” shows the clock toggling duration during 10 ns clock period. For future changes you can directly edit these numbers in this file or you can again repeat the steps from 6 -9.



1. Re run synthesis and then run implementation.
2. Expand implemented design and select “Report Timing constraint”. A window like following means your design is meeting the timing constraints set by you. If you see any numbers in red color in front of any timing parameter in “Design Timing summary” then you will have to modify your design or reduce the clock frequency in the “const.xdc” file. Your design clock period can be “worst negative slack + Worst hold Slack”.

